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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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Driggs, Lucas, Brubaker & Hogg Co., L.P.A.  
8522 East Avenue  
Mentor, OH 44060

EXAMINER

ALCALA, JOSE H

ART UNIT	PAPER NUMBER
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2827

DATE MAILED: 11/25/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

# Office Action Summary

Application No.

09/778,702

Applicant(s)

BHATT ET AL.

Examiner

Jose H Alcala

Art Unit

2827

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

## Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

## Status

- 1) ☒ Responsive to communication(s) filed on 12 July 2002.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

## Disposition of Claims

- 4) ☒ Claim(s) 9-21 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 9-21 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

## Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 07 February 2001 is/are: a) ☐ accepted or b) ☒ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☒ The proposed drawing correction filed on 10 July 2002 is: a) ☐ approved b) ☒ disapproved by the Examiner.  
If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

## Priority under 35 U.S.C. §§ 119 and 120

- 13) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).  
a) ☐ All b) ☐ Some \* c) ☐ None of:  
1. ☐ Certified copies of the priority documents have been received.  
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.  
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).  
\* See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).  
a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

## Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) \_\_\_\_\_
- 4) ☐ Interview Summary (PTO-413) Paper No(s). \_\_\_\_\_
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: \_\_\_\_\_

## DETAILED ACTION

### *Drawings*

1. The proposed drawing correction and/or the proposed substitute sheets of drawings, filed on 7/10/02 have been dissaproved. The changes made to the drawings to show the embodiment where the line width is approximately less than the diameter of said filled plated through hole, and the changes made in order to show the circuitry having an aspect ratio greater than about 1, are approved. However, the drawings are still improperly crosshatched. It is pointed out that the crosshatching pattern of the dielectric substrate and the filler material inside the through hole, should be selected from those shown on page 600-81 of the MPEP based on the material of the part. See also 37 CFR 1.84(h)(3) and MPEP 608.02.

A proper drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The correction to the drawings will not be held in abeyance.

### *Claim Objections*

2. Claim 21 is objected to under 37 CFR 1.75(c), as being of improper dependent form for failing to further limit the subject matter of a previous claim. Applicant is required to cancel the claim(s), or amend the claim(s) to place the claim(s) in proper dependent form, or rewrite the claim(s) in independent form. The limitations added in claim 21, are merely product by process limitations, which add only the process steps

for making the invention, which are not germane to the invention, and are not adding any structure to the independent claim 11.

***Claim Rejections - 35 USC § 112***

3. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4. Claims 9-21 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

It is pointed out that the amendments to claims 9 and 10, and new claim 21, all include product by process limitations. If the product in the product-by-process claims are the same as or obvious from a product of the prior art, the claims are unpatentable even though the prior product was made by a different process. See *In re Thorpe*, 227 USPQ 964,966 (Fed.Cir 1985). A "product by process" claim is directed to the product per se, no matter how actually made, *In re Brown*, 173 USPQ 685; *In re Luck*, 177 USPQ 523; *In re Fessmann*, 180 USPQ 324; *In re Avery*, 186 USPQ 161; *In re Wertheim*, 191 USPQ 90 (209 USPQ 554 does not deal with this issue); *In re Marosi et al*, 218 USPQ 289; and particularly *In re Thorpe*, 227 USPQ 964, all of which make it clear that it is the patentability of the final product per se which must be determined in a "product by process" claim, and not the patentability of the process, and that an old or obvious product produced by a new method is not patentable as a product, whether claimed in "product by process" claims or not. Note that applicant has the burden of

proof in such cases, as the above case law makes clear. Furthermore, any intermediate structure will not be given patentable weight, just the final product.

Regarding Claim 9, it is not clear from the claim which elements are part of the final product, and which of them are just intermediate elements used in the process of making the wiring board. For example in lines 1-2, it is recited: "at least one filled through hole" and then in lines 3 and 4, it is recited: "depositing a seed layer on a planar surface of said dielectric substrate and on a surface defined by a hole through said dielectric substrate". It is unclear if the through hole is filled, how can a seed layer be deposited on a "surface defined by a hole". One further example of the inconsistencies included in the amendment to the claim can be found in lines 2 and 5. Line 2 recites a "plated through hole" and then in line 5, it recites: "depositing electrically conductive plating", making it unclear if this is a second plating, and where it is exactly located in the final structure. For examining purposes, patentable weight is only given to the final product, as best understood by the examiner.

Regarding Claim 10, it is not clear from the claim which elements are part of the final product, and which of them are just intermediate elements used in the process of making the wiring board. For example in lines 1-2, it is recited: "at least one filled through hole" and then in lines 3 and 4, it is recited: "depositing a seed layer on a planar surface of said dielectric substrate and on a surface defined by a hole through said dielectric substrate". It is unclear if the through hole is filled, how can a seed layer be deposited on a "surface defined by a hole". One further example of the inconsistencies included in the amendment to the claim can be found in lines 2 and 5. Line 2 recites a

"plated through hole" and then in line 5, it recites: "depositing electrically conductive plating", making it unclear if this is a second plating, and where it is exactly located in the final structure. For examining purposes, patentable weight is only given to the final product, as best understood by the examiner.

Regarding Claim 12, it is not clear how the circuitry having line width approximately less than the diameter of the through hole can include a pad, which has to have at least the diameter of the through hole. In order to avoid any confusion, the pad cannot be part of the circuitry, but a separate element.

Regarding Claims 18-20, it is not clear if the circuitry is on top of the layer of dielectric material or if it is disposed on top of the dielectric substrate and covered by the layer of dielectric material, or both. If there is a second circuitry, it should be labeled differently, as for example: second circuitry.

Regarding Claim 21, it is not clear from the claim which elements are part of the final product, and which of them are just intermediate elements used in the process of making the wiring board. For example in lines 3 and 4, it is recited: "depositing a seed layer on a planar surface of said dielectric substrate and on a surface defined by a hole through said dielectric substrate", while in the independent claim 11, lines 1-2, it is recited: "at least one filled through hole". It is unclear if the through hole is filled, how can a seed layer be deposited on a "surface defined by a hole". One further example of the inconsistencies included in the new claim can be found in line 5. Independent claim 11, recites a "plated through hole" in line 2, and then claim 21 recites in line 5: "depositing electrically conductive plating", making it unclear if this is a second plating,

and where it is exactly located in the final structure. For examining purposes, patentable weight is only given to the final product, as best understood by the examiner.

***Claim Rejections - 35 USC § 103***

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

6. Claims 9-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Jones et al. (US Patent No. 5,097,593) in view of Lan et al. (US Patent No. 5,906,042). As best understood by the examiner:

Regarding Claim 9, Jones teaches a printed wiring board (Reference Number 10) comprising a dielectric substrate (Reference Number 11), at least one plated through hole (Reference number 12) having an outside diameter, and circuitry having circuit lines (Reference numbers 14,32) on said dielectric substrate connecting to said plated through hole, said circuitry having a line width approximately equal to or less than the diameter of said filled plated through hole.

The limitations that the board is: **"formed by the steps of (a) depositing a seed layer on a planar surface of said dielectric substrate and on a surface defined by a hole through said dielectric substrate;(b) depositing electrically conductive plating having a thickness on said planar surface of said dielectric substrate and on said surface defined by said hole to form a subcomposite;(e) filling said hole**

with a filler composition; (d) etching said subcomposite to partially remove said electrically conductive layer and thereby reducing the electrically conductive plating thickness to a minimum thickness of about 0.2 mil (e) removing residual amounts of said filler composition on said subcomposite; and (f) etching said subcomposite to completely remove said electrically conductive plating"; and the limitations that the: "the circuitry is formed by the steps of (g) depositing a seed activator on the surface of said subcomposite including said filler composition; (h) covering said subcomposite with a photoresist and exposing and developing said photoresist to reveal selected areas of said subcomposite including the filler composition; and (i) additively plating electrical circuitry on said selected areas of said subcomposite including circuitry on said filler composition electrically connected to the electrically conductive plating on the surface defined by the hole", are product by process limitations, and are not given patentable weight by the reasons given above.

Jones fails to teach that the through hole is filled. Lan teaches plated through holes (Reference numbers 407 and 408) filled with a conductive material (409 and 410). It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Jones and Lan in order to have the filled plated through holes, to improve the electrical conduction through the circuit board and from the top surface to the bottom surface and to provide a way to increase or decrease the conductivity of it by changing the materials used and their proportions.

Regarding Claim 10, Jones teaches a printed wiring board (Reference Number 10) comprising a dielectric substrate (Reference Number 11), at least one plated through hole (Reference number 12) having an outside diameter, and circuitry having circuit lines (Reference numbers 14,32) on said dielectric substrate connecting to said plated through hole, said circuitry (Reference number 32) having an aspect ratio greater than about .5.

The limitations that the board is: **"formed by the steps of (a) depositing a seed layer on a planar surface of said dielectric substrate and on a surface defined by a hole through said dielectric substrate;(b) depositing electrically conductive plating having a thickness on said planar surface of said dielectric substrate and on said surface defined by said hole to form a subcomposite;(e) filling said hole with a filler composition; (d) etching said subcomposite to partially remove said electrically conductive layer and thereby reducing the electrically conductive plating thickness to a minimum thickness of about 0.2 mil (e) removing residual amounts of said filler composition on said subcomposite; and (f) etching said subcomposite to completely remove said electrically conductive plating";** and the limitations that the: **"the circuitry is formed by the steps of (g) depositing a seed activator on the surface of said subcomposite including said filler composition; (h) covering said subcomposite with a photoresist and exposing and developing said photoresist to reveal selected areas of said subcomposite including the filler composition; and (i) additively plating electrical circuitry on said selected areas of said subcomposite including circuitry on said filler composition electrically**

**connected to the electrically conductive plating on the surface defined by the hole",** are product by process limitations, and are not given patentable weight by the reasons given above.

Jones fails to teach that the through hole is filled. Lan teaches plated through holes (Reference numbers 407 and 408) filled with a conductive material (409 and 410). It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Jones and Lan in order to have the filled plated through holes, to improve the electrical conduction through the circuit board and from the top surface to the bottom surface and to provide a way to increase or decrease the conductivity of it by changing the materials used and their proportions.

Regarding Claim 10, Jones teaches a printed wiring board (Reference Number 10) comprising a dielectric substrate (Reference Number 11), at least one plated through hole (Reference number 12), and circuitry (Reference numbers 14,32) on said dielectric substrate connecting to said plated through hole, and suggests that it is desirable to have but fails to explicitly teach that said circuitry (Reference number 32) has an aspect ratio greater than about 1. Jones fails to teach that the through hole is filled.

Lan teaches plated through holes (Reference numbers 407 and 408) filled with a conductive material (409 and 410). It is suggested by the Jones reference that the circuitry lines can be put very close together (column 4, lines 37-38, 63-64) and that additional lines can be further added (column 4, lines 47-48), and it is well known in the art to put circuitry lines as closely as possible, in order to improve integration.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to make the circuitry having an aspect ratio greater than about 1, in order to improve integration. In addition, it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or working ranges involves only routine skill in the art. See *In re Aller*, 105 USPQ 233. It would have been further obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Jones and Lan in order to have the filled plated through holes, to improve the electrical conduction through the circuit board and from the top surface to the bottom surface and to provide a way to increase or decrease the conductivity of it by changing the materials used and their proportions.

Regarding Claims 12-14, as best understood by the examiner, Jones teaches that said circuitry includes a pad (Reference Number 14) on each of said filled plated through holes.

Regarding Claims 15-17, Jones teaches a layer of dielectric material (Reference Numbers 18) disposed on said dielectric substrate and overlying said circuitry (it is overlying Reference 14, which is part of the circuitry) on said dielectric substrate, said layer of dielectric material having at least one via (Reference number 20) formed therein.

Regarding Claims 18-20, as best understood by the examiner, Jones teaches circuitry (Reference number 32) disposed on said layer of dielectric material.

Regarding Claim 21, the limitations that: **"the filled plated through hole is formed by the steps of (a) depositing a seed layer on a planar surface of said**

dielectric substrate and on a surface defined by a hole through said dielectric substrate; (b) depositing electrically conductive plating on said planar surface of said dielectric substrate and on said surface defined by said hole to form a subcomposite; (c) filling said hole with a filler composition (d) etching said subcomposite to partially remove said electrically conductive layer; (e) removing residual amounts of said filler composition on said subcomposite; and (f) etching said subcomposite to completely remove said electrically conductive plating; and wherein the circuitry is formed by the steps of (g) depositing a seed activator on the surface of said subcomposite including said filler composition; (h) covering said subcomposite with a photoresist and exposing and developing said photoresist to reveal selected areas of said subcomposite including the filler composition; and (i) additively plating electrical circuitry on said selected areas of said subcomposite including circuitry on said filler composition electrically connected to the electrically conductive plating on the surface defined by the hole", are product by process limitations, and are not given patentable weight by the reasons given above.

### ***Response to Arguments***

7. Applicant's arguments filed 7/10/02 have been fully considered but they are not persuasive.
8. Regarding claim 11, applicant argues that: "Jones explicitly limits the aspect ratio possible through practicing his invention to no greater than 1", in the recitation of

column 5, lines 3-9. Examiner respectfully disagrees, and points out that it is suggested by the Jones reference that the circuitry lines can be put very close together (column 4, lines 37-38, 63-64) and that additional lines can be further added (column 4, lines 47-48). Furthermore, it is well known in the art to put circuitry lines as closely as possible, in order to improve integration, making the discovery of the optimum or working ranges be due only to routine skill in the art. See *In re Aller*, 105 USPQ.

Regarding Claims 9,10 and new claim 21, applicant further argues that the new process limitations, which have been found allowable in a previous application, overcome the prior art rejection of Jones in view of Lan. Examiner respectfully disagrees, and points out that the new limitations added to claims 9,10 and new claim 21, are merely product by process limitations, and are not given patentable weight by the reasons given above.

Regarding Claims 12-14, applicant argues that the Jones structure does not teach the pad structure as claimed. Examiner respectfully disagrees, and points out that the dimensions of the pad structure taught by Jones are in such a small scale that the pad diameter can be construed as "about equal the filled plated through hole diameter".

***Conclusion***

9. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

10. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. The following references have some of the elements of the instant claimed invention: Sedberry (US Patent No. 4,897,676) teaches a circuit board having aspect ratio greater than about .5, Odaira et al. (US Patent No. 5,600,103) teaches a circuit board having aspect ratio greater than about 1, and Ahmad et al. (US Patent No. 5,436,412) teaches a circuit board having aspect ratio greater than about 1.

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jose H Alcala whose telephone number is (703) 305-9844. The examiner can normally be reached on Monday to Friday.

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12. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Talbott can be reached on (703) 305-9883. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 305-3431 for regular communications and (703) 305-3431 for After Final communications.

13. Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

JHA

November 18, 2002

  
ALBERT W. PALADINI  
PRIMARY EXAMINER